PATENT APPLICATION
DOCKET NO.: 200208010-1

"EXPRESS MAIL" Mailing Label No..EV331251214US
Date of Deposit.....JULY 30, 2003.....

PHASE DETECTOR FOR A PROGRAMMABLE CLOCK SYNCHRONIZER

PRIORITY UNDER 35 U.S.C. §119(e) & 37 C.F.R. §1.78

[0001] This nonprovisional application claims priority based upon the following prior United States provisional patent application entitled: "*Programmable Clock Synchronizer and Controller Arrangement Therefor,*" Application No.: 60/469,120, filed May 9, 2003, in the name(s) of: Richard W. Adkisson, which is hereby incorporated by reference.

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0002] This application discloses subject matter related to the subject matter disclosed in the following commonly owned co-pending patent applications: (i) "Programmable Clock Synchronizer," filed 07/30/2003; Application No. 10/630,159 ___ (Docket No. 200207722-2), in the name(s) of: Richard W. Adkisson; (ii) "Controller Arrangement for a Programmable Clock Synchronizer," filed 07/30/2003; Application No. 10/630,182 (Docket No. 200207723-1), in the name(s) of: Richard W. Adkisson; (iii) "System and Method for Synchronizing Multiple Synchronizer Controllers," filed ___

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07/30/2003; Application No. 10/629,989 (Docket No. 200207724-1), in the name(s) of: Richard W. Adkisson; (iv) "System and Method for Maintaining a Stable Synchronization State in a Programmable Clock Synchronizer," filed 07/30/2003; Application No. 10/630,297 (Docket No. 200208008-1), in the name(s) of: Richard W. Adkisson; and (v) "System and Method for Compensating for Skew Between a First Clock Signal and a Second Clock Signal," filed 07/30/2003; Application No. 10/630,317 (Docket No. 200208009-1), in the name(s) of: Richard W. Adkisson, all of which are incorporated by reference herein.

BACKGROUND

[0003] Digital electronic systems, e.g., computer systems, often need to communicate using different interfaces, each running at an optimized speed for increased performance. Typically, multiple clock signals having different frequencies are utilized for providing appropriate timing to the interfaces. Further, the frequencies of such clock signals are generally related to one another in a predetermined manner. For example, a core or system clock running at a particular frequency (F_C) may be utilized as a master clock in a typical computer system for providing a time base with respect to a specific portion of its digital circuitry. Other portions of the computer system's digital circuitry (such as a bus segment and the logic circuitry disposed thereon) may be clocked using timing signals derived from the master clock wherein the derived frequencies (F_D) follow the relationship: $F_C/F_D \geq 1$.

signals are generated by the core clock synchronizer controller 124 for transmission to the bus clock synchronizer 122 so that both synchronizer controllers may be appropriately synchronized. Further, a configuration interface 126, labeled as SYNC_Config in FIG. 1, is provided as part of the programmable synchronizer system 100 for configuring the core clock synchronizer controller 124 so that it may be programmed for different skew tolerances, latencies and modes of operation. In one embodiment, the configuration interface 126 may be implemented as a register having a plurality of bits. In another embodiment, a memory-based setting, e.g., EPROM-stored settings, may be provided as a SYNC configuration interface.

[0020] Additional details regarding the various sub-systems described hereinabove may be found in the following commonly owned co-pending patent applications: (i) "Programmable Clock Synchronizer," filed 07/30/2003; Application No. 10/630,159 (Docket No. 200207722-2), in the name(s) of: Richard W. Adkisson; (ii) "Controller Arrangement for a Programmable Clock Synchronizer," filed 07/30/2003; Application No. 10/630,182 (Docket No. 200207723-1), in the name(s) of: Richard W. Adkisson; (iii) "System and Method for Synchronizing Multiple Synchronizer Controllers," filed 07/30/2003; Application No. 10/629,989 (Docket No. 200207724-1), in the name(s) of: Richard W. Adkisson; (iv) "System and Method for Maintaining a Stable Synchronization State in a Programmable Clock Synchronizer," filed 07/30/2003; Application No. 10/630,297 (Docket No. 200208008-1), in the name(s) of: Richard W. Adkisson; and (v) "System and Method for Compensating for

Skew Between a First Clock Signal and a Second Clock Signal," filed 07/30/2003 ; Application No. 10/630,317 (Docket No. 200208009-1), in the name(s) of: Richard W. Adkisson, all of which are incorporated by reference herein.

[0021] As set forth above and in the cross-referenced U.S. patent applications, the synchronizer system 100 may be programmed for different skew tolerances and latencies, so that data transfer at high speeds can proceed properly even where there is a high skew or requirement of low latency. Further, the synchronizer system 100 can operate with any two clock domains having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$.

[0022] FIG. 2 depicts one embodiment of a phase detector 200 operable to detect phase differences between the clocks used in the synchronizer system 100. Accordingly, it is functionally analogous to the phase detector block 130 shown in FIG. 1. In general, the phase detector 200 employs the rising and falling edges of the core_clock c 106' to sample the bus_clock b 108'. In one implementation, the bus_clock b 108' is sampled by at least one first flip flop (FF) clocked on the rising edge of the core_clock c 106'. As illustrated, flip flops 204 and 206 sample the bus_clock b 108' with the rising edge of the core_clock c 106'. By employing two flip flops for sampling, the phase detector 200 is operable to decrease metastability. Flip flop 204 asserts the sampled bus_clock b 108' signal as a cr_ff signal 208 which is sampled by the flip flop 206 and asserted as a pd_b_cr signal 210.

[0025] The pd_b_cr signal 210 and the pd_b_cf signal 222 are forwarded to the core clock synchronizer controller 124 and, in particular, a cycle and sequence generator and a skew state detector of the core clock synchronizer controller 124 in order to compensate for skew. The cycle and sequence generator and skew state detector receive the pd_b_cr signal 210 and the pd_b_cf signal 222 by registering the signals several times and detecting a one-to-zero transition on the pd_b_cr registers or a zero-to-one transition on the pd_b_cf registers. The detection may be registered N+1 times, wherein, for example, N+1 is 5 if 5:4 is the largest ratio detected. Taps are selected off the registers and the "zero tap" is selected from these registers depending on the sync_ratio signal provided by the bus clock synchronizer controller 122. Typically, the zero point is asserted by the skew state detector as a pd_z signal. Further information regarding the pd_b_cr and pd_b_cf signals in relation to the core clock synchronizer controller may be found in the aforementioned U.S. patent applications entitled "System and Method for Maintaining a Stable Synchronization State in a Programmable Clock Synchronizer," filed 07/30/2003; Application No. 10/630,297 (Docket No. 200208008-1), in the name(s) of: Richard W. Adkisson; and "System and Method for Compensating for Skew Between a First Clock Signal and a Second Clock Signal," filed 07/30/2003; Application No. 10/630,317 (Docket No. 200208009-1), in the name(s) of: Richard W. Adkisson.

[0026] FIG. 3 depicts a timing diagram 300 associated with a portion of the phase detector embodiment 200 of FIG. 2,